nology has been studied. Experimental results show that the He plus RPN process provides better characteristics in reducing the gate current and thickness of gate dielectric films for a thinner gate oxide in the 18–22 Å range. In addition, He can drive enough nitrogen into the top of the gate oxide to form a stoichiometric nitrided layer, thus preventing the gate dielectric films from being damaged under a high-density plasma environment.

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High power X-band (8.4 GHz) SiGe/Si heterojunction bipolar transistor

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A high-performance double-mesa type Si/SiGe/Si power HBT at X-band (8.4 GHz) frequency is demonstrated. Under continuous wave operation, a single 20-finger common-base Si/$Si_{0.75}Ge_{0.25}$/Si ($2 \times 10\,\mu m^2$ of each emitter finger) HBT has an output power of 27.4 dBm and an associated power gain of 7 dB at peak PAE of 32.3%. These parametric values represent the state-of-the-art power performance of SiGe-based HBTs.

Introduction: The successful development of high-speed SiGe-based HBTs [1, 2] has provided the opportunity to integrate RF/microwave circuits and CMOS low-power circuitry on a single chip in next-generation communication units. However, the development of high power Si/SiGe/Si HBTs for this application, and others, has only received limited attention [3]. Si/$Si_{1-x}Ge_x$/Si HBT structure designs optimised for high breakdown voltages, which are required for high-power applications, usually set a severe limit for the frequency response of the device. As a result, the published results on SiGe-based microwave power HBTs have only been limited to low-frequency ranges, such as the L-, S- and C-bands. To operate SiGe/Si HBTs at X-band and higher frequencies with high performance (high output power, high power gain and high power added efficiency, PAE), device structures have to be further optimised by considering the trade-off between high frequency response and high breakdown voltages.

In this Letter, we report the performance characteristics of large-area Si/SiGe/Si HBTs with high-breakdown voltages developed for X-band power applications. The base-collector breakdown voltage (BV_{CBO}) in these devices is as high as 26 V and the small-signal power gain (8.4 GHz) is over 11 dB. Under continuous wave operation at 8.4 GHz, the device output power and the associated power gain at a peak PAE of 32.3% are 27.4 dBm and 7 dB, respectively.

emitter cap	Si	n+	P	$2x10^{19}cm^{-3}$	150 nm
emitter	Si	n	P	$1x10^{18}cm^{-3}$	100 nm
spacer	$Si_{0.75}Ge_{0.25}$	i			5 nm
base	$Si_{0.75}Ge_{0.25}$	p+	B	$8x10^{19}cm^{-3}$	20 nm
spacer	$Si_{0.75}Ge_{0.25}$	i			5 nm
collector	Si	n-	P	$3x10^{16}cm^{-3}$	500 nm
sub-collector	Si	n+	P	$2x10^{19}cm^{-3}$	1000 nm
substrate	Si(100)	p-		$1x10^{12}cm^{-3}$	540 μm

a

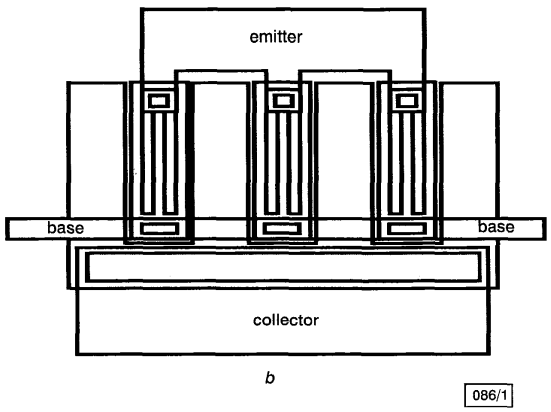

Fig. 1 *Schematic diagram of Si/SiGe/Si double heterostructure HBT and layout of six-finger ($2 \times 30\,\mu m^2$) common-base HBT showing distributed feature*

a Schematic diagram
b Layout of six-finger HBT
Total emitter area of 20-finger common-base HBT is $1560\,\mu m^2$

Device design and fabrication: The design of the *n-p-n* Si/SiGe/Si HBTs was initiated with the heterostructure design and an optimised layout, taking into consideration the requirements for high power handling capability, thermal stability and high-frequency operation. A detailed description of the most important factors for the HBT design can be found in our previous publication [3]. A schematic diagram of the heterostructure grown by one-step CVD is shown in Fig. 1*a*. A 20 nm $Si_{0.75}Ge_{0.25}$ layer was incorporated in the heterostructure as the active base region with a *p*-type doping level of $8 \times 10^{19}\,cm^{-3}$. These parameters ensure a short transit delay across the base layer with a low base resistance. The thick and lightly doped ($3 \times 10^{16}\,cm^{-3}$) collector layer ensures high device breakdown voltages and is favourable for achieving high f_{max} [3]. The layout of a six-finger (each of size $2 \times 30\,\mu m^2$) common-base HBT is illustrated in Fig. 1*b*. In this layout, every two emitter fingers are grouped in a subcell to form a common contact area at the end of the fingers and a 10 μm wide collector metal stripe is inserted in between the two subcells. The total emitter area of a 20-finger device, including the via-hole contact area in each subcell, is $1560\,\mu m^2$. This distributed layout reduces the parasitic collector resistance of this large-area device and greatly assists heat dissipation from the centre of the device. The heterostructures were fabricated into double-mesa type HBTs using standard

photolithography, dry/wet etching, PECVD and e-beam evaporation techniques. Details of this procedure have been described in [4].

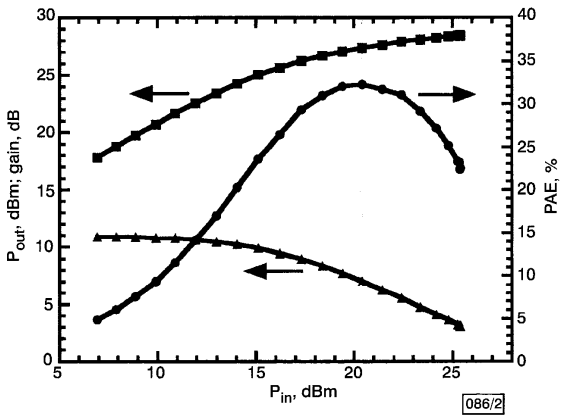

Fig. 2 *Power performance of $Si/Si_{0.75}Ge_{0.25}/Si$ HBT biased under class A operation*

—■— P_{out}
—▲— gain
—◆— PAE

Device performance: The measured base-collector breakdown voltage (BV_{CBO}) is ~26 V and the open-base collector-emitter breakdown voltage (BV_{CEO}) is ~23 V. Although the actual base layer of these devices is only 20 nm thick, no punch-through was observed before the avalanche breakdown occurred. These are the highest breakdown voltages that have been achieved for SiGe-based HBTs. Our study has shown that although the strained $Si_{1-x}Ge_x$ has a smaller bandgap than Si, high breakdown voltages can still be obtained by careful adjustment of the collector doping level. No collapse in the current gain was observed at any collector current level, indicating the excellent heat dissipation capability of the device. The measured small-signal power gain (at 8.4 GHz) at moderate current levels is > 11 dB. The large-signal performance of the device was tested on-wafer with no special heat dissipation or external ballast resistors involved. Under continuous wave operation, biased at class A mode (V_{EB} = –1.48 V, V_{CB} = 7 V), the optimum source and load impedance were found to be Γ_S = 0.82∠180° and Γ_L = 0.83∠150°, respectively, and no oscillation was observed during the measurements. Both matching points are very close to the edge of the Smith chart, indicating the low input and output impedance of this large device. The large value of the bias voltage V_{CB} that can be applied is due to the high breakdown voltages of the devices. Fig. 2 shows the output power, power gain and PAE as a function of input power, measured at 8.4 GHz. The output power at the peak value of PAE (32.3%) is 27.4 dBm (550 mW) with an associated power gain of 7 dB. A high power-gain is favourable for implementing high-power and high-efficiency amplifiers since multiple stages in the amplifier circuit will lower the overall efficiency. The superior performance demonstrated here results from a very low base resistance (R_B), high device breakdown voltages (BV_{CBO} and BV_{CEO}) and good thermal stability of the device at very high power levels. The overall performance characteristics of the $Si/Si_{0.75}Ge_{0.25}/Si$ HBT developed in this study are, to our knowledge, the best among those reported for X-band operation [3, 5, 6].

In conclusion, a double-mesa type $Si/Si_{0.75}Ge_{0.25}/Si$ HBT with a 20 nm base layer has been realised, which exhibits the largest breakdown voltages (BV_{CEO} = 23 V and BV_{CBO} = 26 V), the highest power gain, 7 dB, and the highest output power of 27.4 dBm at the peak value of PAE (32.3%) under class A operation at 8.4 GHz. The large breakdown voltages were achieved by incorporating a lightly doped collector layer and the excellent power performance results from a combination of device heterostructure design and optimised layout, good material quality and optimised processing techniques.

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Symmetric bulk charge linearisation in charge-sheet MOSFET model

T.L. Chen and G. Gildenblat

An accurate, simplified version of the charge-sheet MOSFET model is developed using symmetric linearisation of the bulk charge as a function of surface potential. The resulting MOSFET model satisfies the Gummel symmetry condition and is verified by comparison with the exact results.

Compact MOSFET models used in circuit simulators are often developed with the help of bulk charge linearisation [1]. This leads to simplified and computationally efficient equations of the I-V characteristics and makes possible closed-form evaluation of the intrinsic charges and capacitances. The well-known disadvantage of this approach is a violation of the Gummel symmetry test [1]. We note in passing that there are numerous other mechanisms for the loss of the Gummel symmetry [2].

The purpose of this Letter is to introduce an alternative linearisation scheme for the bulk charge as a function of the surface potential which has all the advantages of the original method [1] but passes the Gummel symmetry test. To separate the linearisation problem from the other aspects of the MOSFET model development we present symmetric linearisation within a context of the charge-sheet model [3]. For this model exact analytical expressions for the drain current and terminal charges are readily available [3, 4], which enables unambiguous evaluation of the accuracy of the symmetric linearisation approach.

Let ϕ_s, ϕ_d denote the surface potentials at the source and drain ends of the MOSFET channel. Define the 'midpoint' as a point with the surface potential $\phi_m = (\phi_s + \phi_d)/2$ and set

$$q_b(\phi) \simeq q_b(\phi_m) + \left(\frac{dq_b}{d\phi}\right)_{\phi=\phi_m} (\phi - \phi_m) \qquad (1)$$

where $q_b(\phi)$ is the absolute value of the bulk charge per unit channel area corresponding to the surface potential ϕ. The absolute